REMARKS

Summary of Office Action

Claims 1-7, 11, 12, and 16-19 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura (US Pub. No. 2001/0002829) in view of Chiang (U.S. Pat. No. 6,271,822).

Claims 8, 9 and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Chiang as applied to claims 1-7, 11, 12, and 16-19 above, and further in view of Applicant's alleged admission of prior art.

Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Chang as applied to claims 1-7, 11, 12, and 16-19 above, and further in view of Gooding et al. (US Pat. No. 4,580,265).

Summary of Amendment

None of the claims has been amended at this time. Claims 1-9, 11, 12, 14-20 are pending for consideration.

All Claims Comply with §103

Claims 1-7, 11, 12 and 16-19 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura in view of Chiang, a newly cited art. Claims 8, 9 and 20 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Chiang, and further in view of Applicant's alleged admission of prior art. Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Nishimura, in view of Chang, and further in view of Gooding et al. Applicants respectfully traverse these rejections

for the following reasons.

The basis for the above rejection is based on the allegation that "Nishimura teaches in FIG. 8 where a two port polarity inverter can be used and further, each inverter has two ports." (OA: p. 3, ll. 5-6.) As reproduced below for convenience, FIG. 8 of Nishimura does not teach a two port polarity inverter as alleged in the Office Action.

FIG. 8A

n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Xn	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Yn	H	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L
Zn	H	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L

FIG. 8B

n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Xn	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Yn	H	H	H	H	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L
Zn	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L

FIG. 8C

n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Xn	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Yn	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	L
Zn	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L

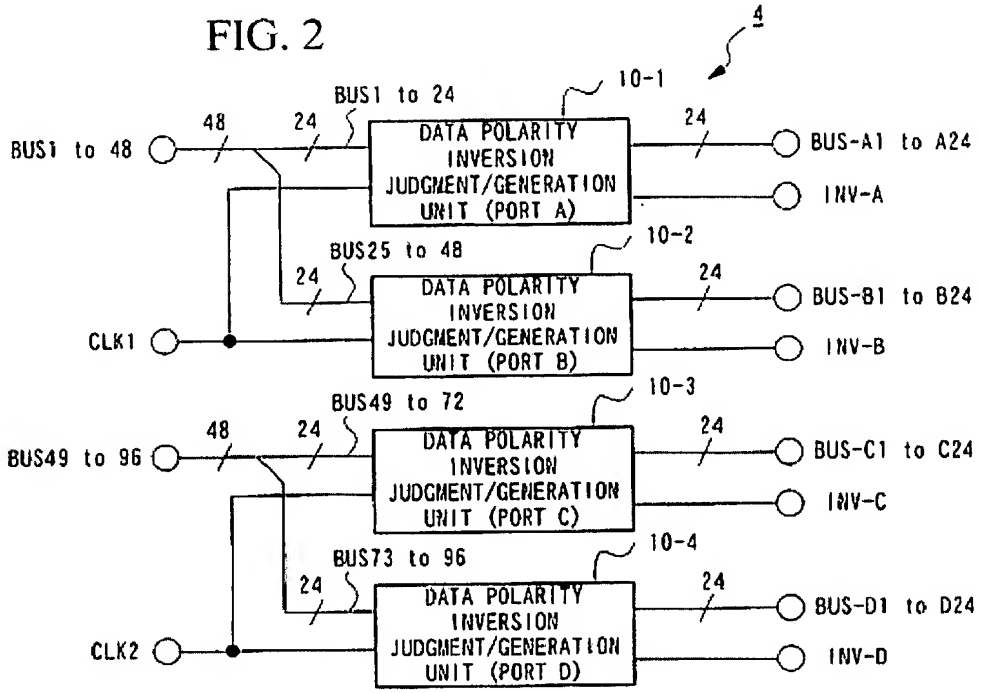
FIG. 8D

n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Xn	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Yn	H	H	H	H	H	H	H	H	H	L	L	L	H	H	H	L	L	L	L	L	L	L	L	L
Zn	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L

Rather, FIG. 8A-D shows the effects obtained by the first embodiment shown in FIG. 1 of Nishimura. (Nishimura: p. 2, para. [0032].) There is no teaching or suggestion of a two port polarity inverter in FIG. 8 of Nishimura as alleged in the Office Action. To the extent that the allegation is directed to FIG. 2 of Nishimura, which is the only figure that shows a multi-port inverter structure, Applicants submit the following comments.

Claim 1 recites, in part, "a first data polarity inversion driver determining whether a first data transition has occurred in a first set of data" and "a second data polarity inversion driver determining whether a second data transition has occurred in a second set of data," wherein the first set of data is odd-numbered bits and the second set of data is even-numbered bits. Nishimura fails to teach at least these features. FIG. 2 of Nishimura is reproduced and annotated below for convenience.

FIG. 2



As shown, FIG. 2 of Nishimura shows a 4-port data inversion circuit, not a 2-port data inversion circuit as alleged in the Office Action. There is no basis for alleging that Port A (10-1) and Port B (10-2) makes up "one polarity inverter" to arrive at a "two port polarity inverter" as Nishimura describes each of the ports (Ports A-D) as receiving one-fourth of the total data lines. More importantly, the circuit shown in FIG. 2 of Nishimura is related to a polarity circuit, not a first

and second polarity ***inversion*** circuit as claimed.

A polarity signal is not the video data voltage value applied to the liquid crystal cell but the polarity value (i.e., positive or negative). The polarity value is generally reversed to eliminate the effect of the previous voltage data on the liquid crystal cell. While Nishimura teaches using inverse polarity signals to reverse the polarity of the video signals present on each data line, Nishimura fails to teach a first and second polarity inversion circuit that generates an inversion signal based on the data transition information that determines if the polarity signal should be inverted in the first place.

However, even if, *in arguendo*, the pair of the ports in Nishimura are construed as a "two port polarity inverter" as alleged in the Office Action, Nishimura still fails to teach "a first data polarity inversion driver determining whether a first data transition has occurred in a first set of data" and "a second data polarity inversion driver determining whether a second data transition has occurred in a second set of data," wherein the first set of data is "odd-numbered bits" and the second set of data is "even-numbered bits." Nishimura teaches that the data polarity inversion judgment/generation units (Ports A-D) determine whether to invert the data based on the number of bits having different values among each of the 24 bit blocks of data. (Nishimura: p. 4, para. [0053].) Accordingly, Nishimura fails to teach or even suggest a first data polarity inversion driver determining whether a first data transition has occurred in the odd-numbered bits of data and a second data polarity inversion driver determining whether a second data transition has occurred in the even-numbered bits of data.

Looking, then, to the secondary reference, Chiang teaches a liquid crystal display (LCD)

driving circuit including a digital gamma correction and inversion circuit 221. Chiang teaches that

> ...the purpose of the selective polarity inversion process is to make neighboring lines in the video display to be opposite in polarity; for instance the odd-numbered lines (1st, 3rd, 5th, ...lines) are positively polarized, while the even-numbered lines (2nd, 4th, 6th, ...lines) are negatively polarized. (Col. 5, ll. 28-35.)

This section of Chiang only teaches that the odd-numbered bits are inverted with respect to the even-numbered bits ***every time***. Chiang does not teach or suggest a first and second polarity inversion driver as recited in claim 1 nor does Chiang teach determining whether a first or second data transition has occurred in the odd-numbered bits or the even-numbered bits of the data. Accordingly, Chiang does not cure the deficiencies of Nishimura.

More importantly, Nishimura and Chiang cannot be combined in the manner alleged in the Office Action because Nishimura's invention is meant to replace the inefficiencies of the prior art like Chiang's invention. That is, while Chiang teaches that every odd-numbered bit of the video data is inverted with respect to every even-numbered bit of the video data, Nishimura teaches, by contrast, inverting all data in the 24-bit block if the data polarity inversion judgment/generation unit (e.g., 10-1) determines that enough of the bits have different values. (Nishimura: p. 4, para [0053], ll. 11-15.) This is evidenced by FIGs. 8A-8D in Nishimura (see above) that show blocks of data bits (i.e., 1-24) having low (L) or high (H) inversion signals rather than (L) and (H) alternating with each other as would be shown in accordance with Chiang's teachings.

Courts have held that "prior art must be considered in its entirety, i.e., as a whole,

including portions that would lead away from the claimed invention." W.*L. Gore & Associates, Inc. v. Garlock, Inc.* 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) (see also MPEP §2141.02) (emphasis added). The courts have held that it is ***improper to combine*** references where the ***references teach away*** from their combination. *In re Grasselli*, 713 F.2d 731, 743, USPQ 769, 779 (Fed. Cir. 1983) (see also MPEP §2145(X)(D)(2)). Furthermore, as stated in MPEP §2143.01, "[i]f proposed modification would render the prior art invention being modified ***unsatisfactory for its intended purpose***, then there is no suggestion no motivation to make the proposed modification," citing to *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In the present case, Nishimura's multi-port data polarity inversion judgment/generation units invert signals based on the determination of value differences within a block of 24 bits of data. This intended purpose would be destroyed if Nishimura is modified by Chiang in the manner alleged because Chiang teaches inverting all odd-numbered bits in relation to all even-numbered bits. Therefore, not only does Nishimura and Chiang, whether taken individually or in combination, fail to teach all of the features of claim 1, but Nishimura cannot be modified by Chiang's teaching as alleged for the reasons explained above.

Independent claim 11 recites, in part, the steps of "inputting the first and second sets of data to the first and second data polarity inversion drivers, respectively," "determining a number of first and second data transitions in the first and second sets of data, respectively," and "inverting a polarity of the first and second sets of data in accordance with the determined results," wherein the first set of data is odd-numbered bits and the second set of data is even-numbered bits. As explained above, Nishimura and Chiang both fail to teach determining a

number of first and second data transitions in the odd-numbered bits and the even-numbered bits and inverting the polarity of the odd-numbered and even-numbered bits based on the determination. Accordingly, Nishimura and Chiang, whether taken individually or in combination, fail to teach all the features of claim 11. Moreover, Nishimura and Chiang cannot be combined as explained above.

Independent claim 16 recites a 2-port data polarity inverter including, in part, "an odd data polarity inversion driver" to invert the polarity when a first transition is detected in the odd-numbered bits and "an even data polarity inversion driver" to invert the polarity when a second transition is detected in the even-numbered bits. As explained above, Nishimura and Chiang both fail to teach or suggest such features. Accordingly, Nishimura and Chiang, whether taken individually or in combination, fail to teach all the features of claim 16. Moreover, Nishimura and Chiang cannot be combined as explained above.

Dependent claims 2-7, 12 and 17-19 depend from one of independent claims 1, 11, and 16, thereby incorporating all the features of their respective base claim. Accordingly, Nishimura and Chiang, whether taken individually or in combination, fail to teach all the features of claims 2-7, 12 and 17-19 for at least the reasons stated above.

As to claims 8, 9, 14, 15, and 20, the alleged admission of prior art and Gooding et al. fail to cure the deficiencies of Nishimura and Chiang described above. Accordingly, Nishimura, Chiang, alleged admission of prior art, and Gooding et al., whether taken individually or in combination, fail to teach all the features of claims 8, 9, 14, 15, and 20 for at least the reasons stated above. Therefore, Applicants request that the §103 rejections be withdrawn.

CONCLUSION

In view of the foregoing, reconsideration and timely allowance of the pending claims are respectfully requested. Should the Examiner feel that there are any issues outstanding after consideration of the response, the Examiner is invited to contact the Applicants' undersigned representative to expedite prosecution.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

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